AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 1, line 12, with the following amended paragraph:

An FED panel with a conventional FED is illustrated in FIG. 1. A cathode 2 is formed over a substrate 1 with a metal such as chromium (Cr), and a resistor layer 3 is formed over the cathode 2 with an amorphous silicon. A gate insulation layer 4 with a well 4a, through which the bottom of the resistor layer 3 is exposed, is formed on the resistor layer 3 with an insulation material such as SiO_2. A micro-tip 5 formed of a metal such as molybdenum (Mo) is located in the well 4a. A gate electrode 6 with a gate 6a aligned with the well 4a is formed on the gate insulation layer 4. An anode 7 is located a predetermined distance above the gate electrode 6. The ~~gate electrode~~ anode 7 is formed on the inner surface of a faceplate ~~9~~ 8 that forms a vacuum cavity ~~in~~ associated with the substrate 1. The faceplate 8 and the substrate 1 are spaced apart from each other by a spacer (not shown), and sealed at the edges. As for color displays, a phosphor screen (not shown) is placed on or near the anode 7.

Please replace the paragraph beginning at page 4, line 9, with the following amended paragraph:

The above objects and advantages of the present invention will become more apparent by describing in detail preferred embodiments thereof with reference to the attached drawings in which:

FIG. 1 is a sectional view of a conventional field emission device (FED);

FIG, 2 is a plan view of a preferred embodiment of an FED according to the present invention;

FIG. 3 is a magnified view of the portion A of FIG. 2;

FIG. [[4]] 4A is a sectional view taken along line A-A′ of FIG. 3;

FIG. 4B is an alternative sectional view of FIG. 3;

FIGS. 5 through 8B are sectional views illustrating the fabrication processes of an FED according to a preferred embodiment of the present invention;

FIG. 9 is a scanning electron microscope (SEM) photo showing a section of the FED fabricated by the inventive method;

FIG. 10 is a SEM photo showing the configuration of a micro-tip of the FED of FIG. 9; and

FIG. 11 is a SEM photo showing the configuration of the focus gate electrode of the FED fabricated by the inventive method.

Please replace the paragraph beginning at page 4, line 26 and ending on page 5, line 6, with the following amended paragraph:

The present invention will now be described more fully with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. Referring to FIG. 2, which is a plan view of a field emission device (FED) according to the present invention, a cathode 120 and a gate electrode 160 are arranged in a x-y matrix at the center of a substrate 100, and a focus gate electrode 190 that is a feature of the present invention is arranged over the cathode 120 and the gate electrode 160. The cathode 120 and the gate electrode ~~140~~ 160 are

electrically connected to pads 121 and 161, respectively, arranged on the edges of the substrate 100.

Please replace the paragraph beginning at page 5, line 7, with the following amended paragraph:

Portion A of FIG. 2 is enlarged in FIG. 3. As shown in FIG. 3, the focus gate electrode 190 has a focus gate 190a through which the cross-overlapped portion of the cathode ~~130~~ 120 and the gate electrode 160 is exposed. In particular, the gate electrode 160 with the gate 160a is exposed through the ~~post~~ focus gate 190a. The focus gate electrode 190 is located such that the cross-overlapped portion of the cathode 120 and the gate electrode 160, i.e., corresponding to a single pixel, is exposed through its focus gate 190a. The distance between the gate electrode 190 and the pads 121 and 161 are determined in the range of 0.1-15 mm, such that the gate electrode 160 and the cathode 120 are fully covered with the focus gate electrode 190. The focus gate electrode 190 is electrically coupled with an external ground, thereby providing electron emission when an arching occurs with a high voltage. As a result, the underlying layers can be protected from damage.

Please replace the paragraph beginning at page 5, line 19, with the following amended paragraph:

FIG. [[4]] 4A is a sectional view taken long line A-A′ of FIG. 3. Referring to FIG. [[4]] 4A, a cathode 120 is formed over a substrate 100 with a metal such as chromium (Cr), and a resistor layer 130 is formed over the cathode 120 with an

amorphous silicon. A gate insulation layer 140 with a well 140a, through which the bottom of the resistor layer 130 is exposed, is formed on the resistor layer 130 with an insulation material such as SiO_2. Use of the resistor layer 130 is optional. In other words, formation of the resistor layer 130 may be omitted so that the cathode 120 is exposed through the well 140a. Alternatively, the resistor layer 130 can be below the cathode 120, or is formed both over and beneath the cathode 120, as shown in Figure 4B. A micro-tip 150, which is a feature of the present invention, is formed in the well 140a on the resist layer 130 with a metal such as molybdenum (Mo). A micro-tip 150 is a collection of a large number of nano-tips with nano-size surface features. The micro-tip 150 is formed of Mo, W, Si or diamond, or a combination of these materials.

Please replace the paragraph beginning at page 7, line 5, with the following amended paragraph:

Then, a focus gate ~~109a~~ 190a or 190b is formed in the focus gate electrode 190 by photolithography. Referring to FIGS. 7A and 7B, a predetermined photoresist pattern 200a or 200b is formed on the focus gate electrode 190, and portions of the focus gate electrode 190 which are exposed through the photoresist pattern 200a or ~~100b~~ 200b are etched by a general dry or wet etching method using the photoresist pattern 200a or 200b as an etch mask, thereby resulting in the focus gate 190a or 190b in the focus gate electrode 190. FIG. 7A illustrates a configuration in which a plurality of micro-tips 160 are exposed through the same single focus gate 190a, and FIG. 7B illustrates a configuration in which just one micro-tip 150 is exposed through

a single respective focus gate 190a. The thickness of the focus gate insulation layer 191 is in the range of 3-150 μm for the configuration of FIG. 7A, and of 6-50 μm for the configuration of FIG. 7B. In particular, when each gate 160a is exposed through a single respective focus gate 190a, the thickness of the focus gate insulation layer 191 may be in the range of 3-10 μm. Alternatively, when 2-4 gates 160a are exposed through the same single focus gate 190a, the thickness of the focus gate insulation layer 191 may be in the range of 6-50 μm. When a single focus gate 190a corresponds to one pixel or dot defined by a cross-overlapped portion between the gate electrode and the cathode, the thickness of the focus gate insulation layer 191 may be in the range of 10-150 μm.

Please replace the paragraph beginning at page 7, line 24 and ending on page 8, line 2, with the following amended paragraph:

Once the formation of the focus gate 190a or 190b is completed, the photoresist pattern 200a or ~~200~~ 200b is stripped, and the underlying focus gate insulation layer 191 is etched using the focus electrode pattern 190′ as an etch mask. The focus gate insulation layer 191 may be etched by dry etching such as RIE or plasma etching. When a plasma etching method is applied, a gas mixture containing O_2 as a major component, and a fluorine-based gas such as CF_4, SF_6 or CHF_3 may be used as a reaction gas. The gas mixture may be CF_4/O_2, SF_6/O_2, CHF_3/O_2, $CF_4/SF_6/O_2$, $CF_4/CHF_3/O_2$, or $SF_6/CHF_3/O_2$. Alternatively, a gas mixture of O_2 and a chlorine-based gas, for example, Cl_2/O_2, CCl_4/O_2, or $Cl_2/CCl_4/O_2$, can be used as a reaction gas.

Please replace the paragraph beginning at page 8, line 18, with the following amended paragraph:

FIG. 9 is a scanning electron microscope (SEM) photo showing the micro-tip, gate insulation layer, and gate electrode formed on the substrate, and FIG. 10 is a magnified view of the micro-tip of FIG. 9. As shown in FIGS. 9 and 10, the micro-tip as a collection of nano-tips has nano-sized surface ~~feature~~ features, as described previously. As a test result, the gate turn-on voltage of the FED fabricated by the method according to the present invention is reduced by about 20V, and the working voltage (a voltage level at a 1/90 duty ratio and a 60Hz frequency) is lowered by about 40-50V, compared with a conventional FED. The height of the micro-tip and the size of the nano-tips can be varied by adjusting the etching ratios or etching rates of the focus gate insulation layer formed of a carbonaceous polymer, and the micro-tip during the plasma etching, as described previously. FIG. 11 is a SEM photo of the FED illustrating the sharp vertical sidewalls of an opening in the focus gate insulation layer. As a leakage test result, a resistance between the focus gate electrode and the gate electrode is higher than 10 MΩ.